X-1069 US 10/086,129 PATENT Conf. No.: 2232

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IN THE UNITED STATES PATENT OFFICE

Applicant:

David P. Schultz

Assignee:

Xilinx, Inc.

Title:

Method and System for Flexibly Nesting JTAG TAP

Controllers for FPGA-Based System-On-Chip (SoC)

Serial No.:

10/086,129

File Date:

2/28/2002

Examiner:

James C. Kerveros

Art Unit:

2133

Docket No.:

x-1069 US

Conf. No.:

2232

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Alexandria, Virginia 22313-1450

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AMENDMENT IN RESPONSE TO FIRST OFFICE ACTION

Dear Sir:

In response to the first Office Action mailed from the Patent Office on June 28, 2004, please amend the application as follows.

Amendments to the Claims listing begins on page 2 of this paper.

Remarks begin on page 8 of this paper.



Modified 02-03

PTO/SB/21 (01-03)
Approved for use through 9/30/00. OMB 0651-0031
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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	TRANSMITTAL FORM (to be used for all correspondence after initial filing) Mail Stop: AMENDMENT			Application / Conf. No.	10/086,129 / 2232	
				Filing Date	February 28, 2002	
				First Named Inventor	David P. Schultz	
				Examiner Name	James C. KeREGEIVED	
				Art Unit	2133 OCT 0 5 2004	
ł	Express Mail Receipt No.			Patent No.		
Total Number of Pages in This Submission				Attorney Docket Number	X-1069 US	
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Date September/27, 2004			684	Charge any additional fees required/credit any overpayment to our Deposit Account Number: 24-0040		
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